
Controlling a Triac with a phototriac

This application note provides guidelines for proper operation of Triac controlled by means of phototriac. Constraints associated with resistive or inductive loads are discussed and typical circuit recommendations are proposed.

Phototriacs (or opto isolated Triacs) are used to provide isolation between the low level control circuitry (command) and the Triac connected to the AC line. This isolation requirement can be either driven by electrical safety (no hazardous voltage must be accessible to end-user) or by topology constraint (insulated command circuit from a different voltage reference). The phototriac implementation seems at first rather straightforward since no additional power supply is required to drive the Triac gate. However, the use of a phototriac can rapidly raise problems like, among others, electrical fast transients (EFT) withstanding. Confronted with these difficulties, the designer has the option to add a snubber network. Although the circuit design is easily accomplished with relatively few components, the choice of resistor and capacitor values forming this network is often awkward and results from various compromises that can be very time-consuming to achieve. Reviewing this document will help the designer to understand the trade-off that has to be made for an application involving a phototriac as a driver for a power Triac.

The Triac is well known by designers as a semi-conductor device, which is essential in controlling power from an AC source (mains). Specifically designed to operate as a switch in an alternating current power system, the advantages of the Triac are its noiseless operation, its ability to be controlled at anytime and without rebounds, its automatic turn-off when the current reaches zero after the control has been removed, and its ability to stand up to an unlimited number of operating cycles wear.

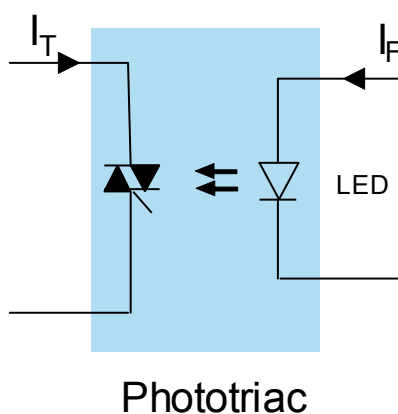
The field of application of the Triac is wide. As a matter of fact, it covers the control of all the equipment operating on alternating current found in home appliances (actuator, pump, lamps, universal motor), building automation (heater, fan) and industrial control (motor drive, starters).

The Triac changes from the off-state to the conducting state when a current or current pulses are applied to the control electrode (gate). Turning on the device can be achieved precisely while synchronizing with the input voltage whereas turn-off occurs when the current passes through zero following the control signal removal.

The Triac is fired by a gate current $I_G > I_{GT}$ whose duration should enable the load current to reach the Triac latching current value (I_L). Thanks to its versatility, a microcontroller is generally used to trigger the Triac.

For some applications, in order to save the cost of a transformer, the choice can be made to connect this microcontroller directly to the line (see AN3168). No hazardous voltage is accessible since there is always a non-conductive interface between control circuit and end-user. However, when additional safety or functional insulation are required, insulated control is preferred. AN4606 and AN4933 give an overview of existing solutions with their respective advantages and drawbacks. An opto-transistor for example allows a DC gate current to be applied and enables control of low RMS current load. For higher RMS current load, and when size and component number prevail, phototriac is still very popular. This is this solution that is developed through the present application note.

A phototriac is composed of a Triac, whose gate is light sensitive, and a led. When a forward current I_F (provided usually by a micro controller unit) flows through the led, photons are generated and transmitted towards Triac junction. If this current is above the led trigger current (I_{FT}), the Triac latches on. It will remain in this “on-state” until current through Triac (I_T) decreases below its holding current (I_H). Once this threshold is passed the Triac returns to a non-conductive state.



A category of phototriac features an additional detector chip that enables triggering only when ac voltage is close to zero. It belongs to the “zero-cross” family of optical Triac driver and, compared to phototriac that lacks this characteristic, contributes to limit surge current at turn-on (mainly an issue on resistive load) and presents less generated noise. Load control with a phase angle is only possible with a non-zero crossing phototriac (also called “random phase”). Conversely, phototriacs with embedded ZVS (zero voltage switching) are appropriate to drive a load in continuous mode.

As specified in many phototriac datasheets, the opto-isolator should not be used to drive a load directly. It is intended to be a trigger device only. Phototriacs are very rarely used as AC switches. There are several reasons why phototriacs are not intended for standalone service.

Some are obvious and can be directly deduced from the datasheet. For example, maximum power dissipation specified is only few hundreds of mW at 25 °C while peak surge current withstanding is around 1 A.

Commutating di/dt , also called $(di/dt)_c$, is a dynamic parameter somewhat difficult to apprehend, and represents an important phototriac weakness that makes this device not suitable to drive a load directly.

This parameter corresponds to the phototriac/Triac behaviour at turn-off. If the slope of the decreasing current is too high and/or if the slope of the reapplied voltage is too high, the device may trigger and the conduction may continue after the zero current crossing point. This non-destructive event is troublesome since the load becomes unmanageable. To get a fair idea of phototriac $(di/dt)_c$ capability, four references of phototriac are measured. Results are collected in [Figure 2](#)

T _J = 25 °C	Datasheet value	(dI/dt) _c (A/ms)		(dV/dt) _c (V/us)	
		+	-	+	-
phototriac 1	Not specified	0.19	0.021	1.81	0.15
phototriac 2	Typ. (dV/dt) _c = 0.2 V/us	0.24	0.04	2.45	0.36
phototriac 3	Not specified	0.02	0.03	0.045	0.19
phototriac 4	Not specified	0.016	0.02	0.05	0.38

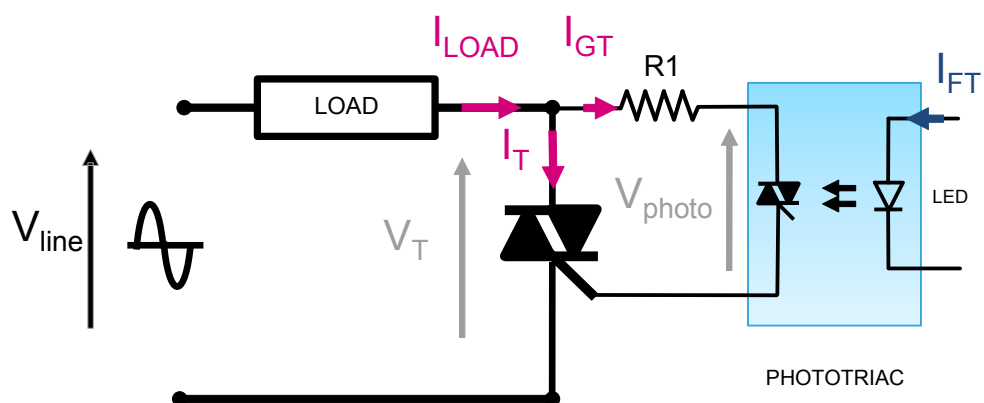
For phototriac 3 and 4, only dI/dt inferior to respectively 0.03 A/ms and 0.02 A/ms will guarantee turn-off (for negative current only). Considering a resistive load (an inductive load would be even more limiting), the maximum load current is given by:

$$I_{RMS} = \frac{T}{2\pi} \times \frac{1}{\sqrt{2}} \times (dI/dt)_c$$

For a 50 Hz supply, a maximum 70 mA resistive load could be controlled by these phototriacs (derating with temperature and safety margin still need to be taken into consideration). Such a low RMS current limits drastically the field of applications opened to phototriac.

It must be reminded that low (dI/dt)_c is not an issue when used in combination with a Triac, since the phototriac is already off when zero current is passed. A commutating dV/dt is seen by the phototriac as a static dV/dt.

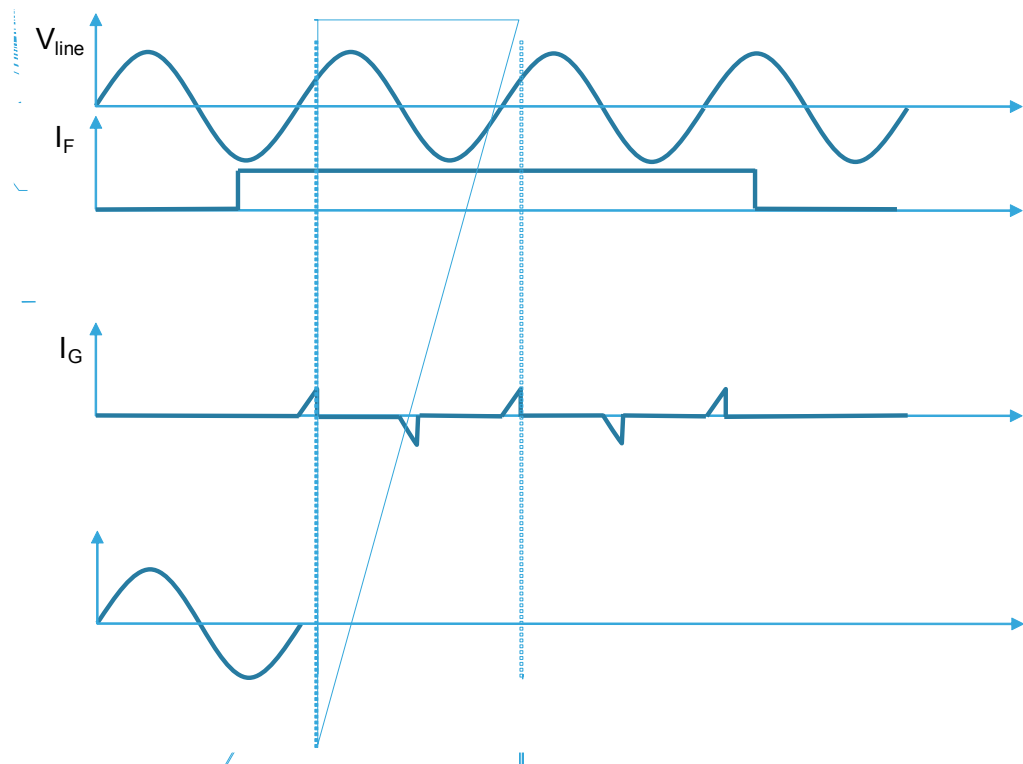
The simplest Triac gating circuit that can be implemented is shown on [Figure 3](#).



Starting with power Triac and phototriac in off state, AC voltage is supplied to the circuit (Figure 4):

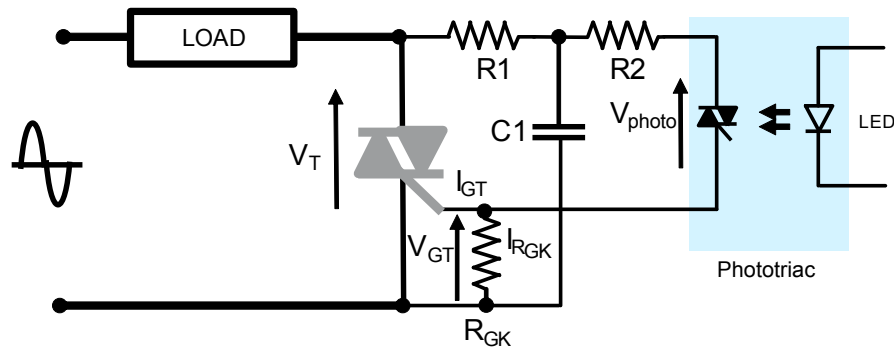
- To drive the phototriac, a current I_F is sourced into the led (1)
- Phototriac switches on when current flowing through the led exceeds I_{FT} . At this time, the gate and the anode of the main Triac are connected together through R1. Due to the voltage difference between anode and gate, a gate current arises in the main Triac (2), triggering it from the blocking state into conducting state (3). Voltage across main Triac drops to a low value (as voltage is now applied to the load, and load current is flowing through the Triac), and consequently current in phototriac declines below its holding current causing phototriac to turn-off. This change to blocking state occurs even if I_{FT} current is still present in the led.
- The power Triac, in conducting mode, switches off at its turn when load current diminishes below holding current at the end of each half sine wave of AC line (4)
- It is re-triggered if I_{FT} is still present through the led (5)

Following this working mode we can conclude that a Triac controlled with a phototriac always uses the quadrants 1 and 3 and never the quadrants 2 and 4.



AC power lines are subjected to fast voltage transients or noise. As phototriacs are connected to the mains, they may trigger accidentally if applied dV/dt oversteps specified static dV/dt (see [Section 3.1](#)).

The previous network ([Figure 3](#)) shows poor noise immunity and must be amended with the schematics shown on [Figure 5](#).



To limit the rate of rise of voltage across the phototriac a capacitor C1 is first placed in parallel with the power Triac (in [Figure 5](#), a highly immune T835-8FP is used). This capacitor cannot be left alone: if the power Triac triggers on when capacitor voltage is near peak ac voltage, a high surge current suddenly runs through the Triac. It will harm device reliability and may even damage it if maximum dI/dt turn-on is exceeded.

A serial resistor R1, placed between C1 and power Triac limits this surge current. This combination of resistor and capacitor connected in series is called a snubber.

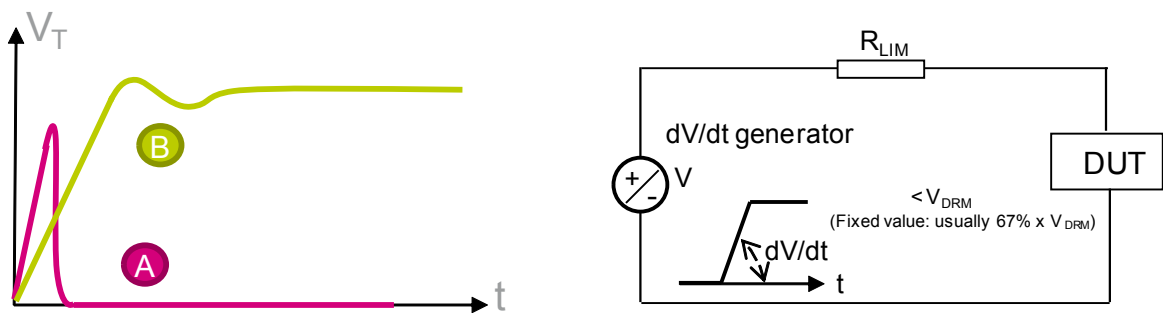
For the same reason, a second resistor R2 is used to restrain C1 current discharge through phototriac in case phototriac switches on when capacitor voltage is close to peak AC voltage.

At last, a resistor R_{GK} between gate and A1 (this terminal is still also called “cathode” as a reference to a Triac formed by two SCR) finalizes the drive circuit. Its purpose is to reduce spurious triggering of the power Triac caused by dV/dt occurring at high temperature.

The benefit brought by a snubber is presented in the subsequent chapter ([Section 3.3.2](#))

This part helps the designer to overcome common pitfalls met when a phototriac is used to control a Triac. Snubber influence on circuit performance is discussed and advices on circuit behavior improvement are given.

Static dV/dt is the maximum rate of off-state voltage rise that a phototriac (or a Triac) is able to withstand without turning on.



As shown on Figure 7, phototriacs have a large range of performance (from 350 V/ μ s up to 5000 V/ μ s). If some reference display good immunity against fast voltage transients, other can suffer from spurious triggering at relatively low static dV/dt and would not fit to applications in noisy environment.

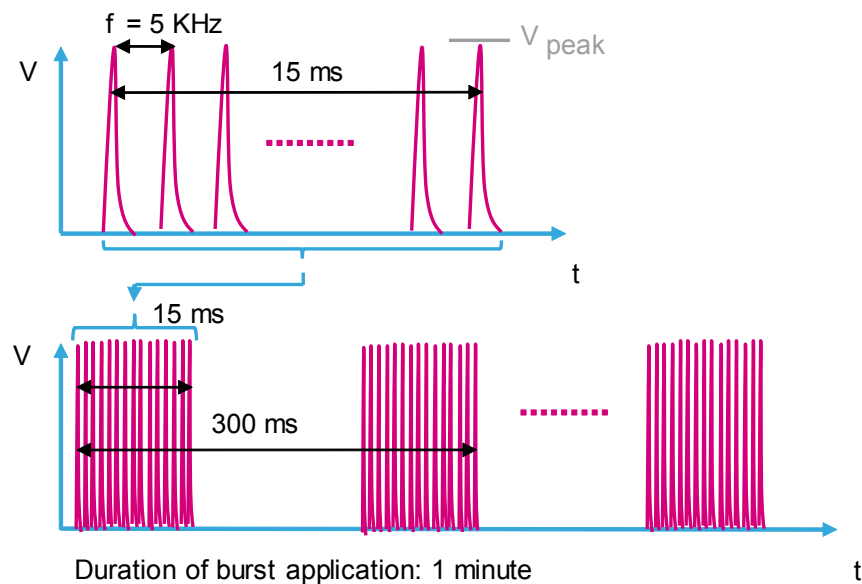
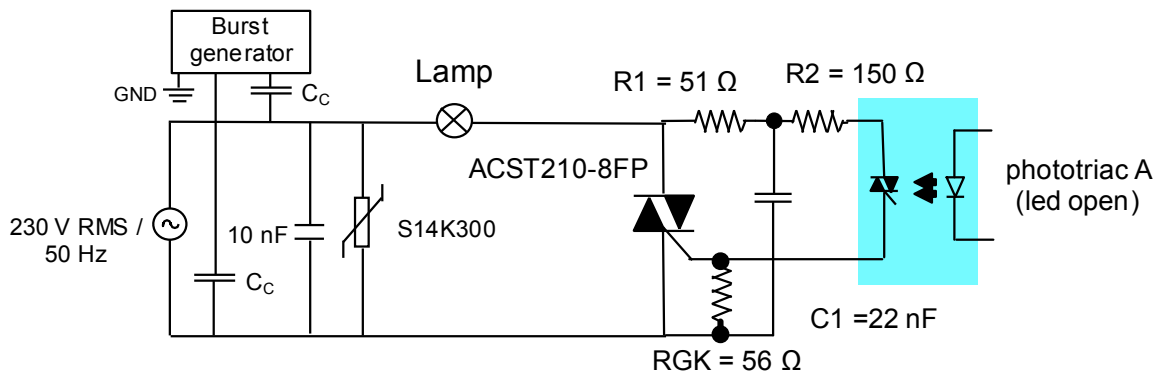
It is interesting to notice that static dV/dt is specified at 25 °C for phototriac and maximum junction temperature (125 °C or 150 °C) for Triac, showing that Triac (power device) is well optimized for use in continuous conduction whereas phototriac is not. In Figure 7, typical static dV/dt of phototriacs is evaluated at 115 °C to mirror application worst conditions.

P/N	Datasheet value (V/us)	dV/dt @ 115°C (Led open) (V/us)	
		+	-
phototriac 1	Min. 1000 V/us @ 25 °C	>5000	>5000
phototriac 2	Min. 600 V/us @ 25 °C	3030	3417
phototriac 3	Min. 600 V/us @ 25 °C	350	370

EFT/bursts refer to the noise generated by electromechanical switch contacts being opened. It creates a burst of low-energy and high frequency spikes that propagate away from the source on power supply and signal lines. Subjected to this burst the phototriac may latch without any command.

The immunity of electrical equipment subjected to fast transient/burst on supply is evaluated according to the test method described in IEC 61000-4-4 standard. Although this test method is different from the one used for static dV/dt (see Figure 6), the values obtained with the two standards are often related (good IEC61000-4-4 specification leads to a high static dV/dt withstanding).

Using the following test set-up (see Figure 8), EFT immunity of phototriac "A" is measured. To better evaluate the influence of the phototriac, an ACST210-8FP is chosen as power Triac. This ACST2 is a sensitive device ($I_{GT} = 10 \text{ mA}$) that provides a high noise immunity level (typically 3 KV) against fast transients. Immunity level is 5 to 10 times higher than the immunity provided by an equivalent standard technology Triac with the same sensitivity.



Two couplings are tested: between line and ground and between neutral and ground. For each coupling, bursts are applied in positive and negative polarity. Results are gathered in Figure 10.

Coupling		V_{peak}			
		L		N	
Polarities		+	-	+	-
ACST210 alone		3.4 kV	4.2 kV	4.1 kV	3.9 kV
ACST210 + phototriac "A"	Without snubber ($R_{GK} = 56$ or 390Ω)	< 1 kV	< 1 kV	< 1 kV	< 1 kV
	With snubber ($R_{GK} = 56$ or 390Ω , $R1 = 51 \Omega$, $R2 = 150 \Omega$, $C1 = 22$ nF)	5.2 kV	5.2 kV	5.2 kV	5.2 kV

A phototriac with low static dV/dt (phototriac A withstands 600 V/ μ s at 25 °C as indicated in the datasheet) deteriorates performance of the driven Triac if it is used without snubber (immunity falls from 3.4 kV to less than 1 KV). To reach the same performance than a Triac alone (3.4 kV and upwards), a snubber is required.

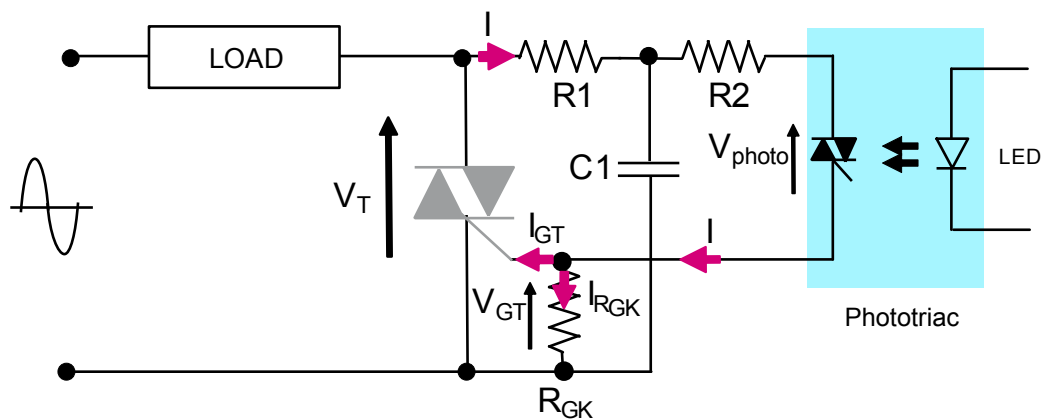
One issue commonly faced on applications using phototriac drive is conducted noise emission. The problem comes from the delay between the zero voltage crossing moment and the time the Triac actually turns on. It occurs specifically on resistive loads where low inductance does not limit high di/dt rate produced by voltage step. Even though the phototriac is triggered on (at the zero cross point of the ac voltage for a phototriac with zero crossing detector chip), the power Triac cannot be switched on until the voltage of the ac line rises high enough to create adequate current in its gate. This requires the presence of sufficient line voltage V_T between A2 and A1. Voltage ripple across Triac before turn-on can lead to electromagnetic interference (EMI) noise above standard limit (for example EN55014 for appliances).

In order to have a thorough grasp of the subject, a high junction temperature Triac, T810T-8FP, well suited to control a resistive load, is used with a phototriac. Starting from circuit shown on [Figure 5](#), the different constraints for proper operation are reviewed.

First, as explained previously in [Section 2.3](#), R_2 must be set to limit the peak capacitor discharge current if phototriac is switched on near the peak ac voltage. For resistive load, where current and voltage are in phase with each other, it is mainly a problem for non-zero crossing phototriacs which can be triggered outside of the zero cross point of the AC voltage, but it could happen as well to zero crossing phototriacs in case of spurious latching. With $V_{line} = 220 V_{RMS}$ and assuming that phototriac maximum surge current is 2 A:

$$R_2 = \frac{V_{line}(peak)}{I_{surge}} = \frac{220 \times \sqrt{2}}{2} = 156 \Omega$$

Secondly, care must be taken to limit maximum voltage V_{TMax} necessary to trigger the Triac. As shown in [Figure 18](#) and [Figure 19](#), voltage ripple across Triac before turn-on can lead to EMI noise above standard limit (EN55014). To evaluate this ripple, it must be remembered that a necessary condition for a Triac to become conductive is to meet its gate requirements (called I_{GT} and V_{GT} in Triac datasheets). The value of maximum line voltage needed to reach the gate specification can be obtained by adding the entire voltage drop across the trigger circuit.



$$V_T = (R1 + R2) \times I + V_{GT} + V_{photo} \quad (1)$$

$$(2) \quad V_{GT} = R_{GK} \times I_{RGK}$$

$$(3) \quad I = I_{GT} + I_{RGK}$$

From (1), (2) and (3):

$$(4) \quad V_T = (R1 + R2) \times I_{GT} + \left(\frac{R1+R2}{R_{GK}} + 1 \right) \times V_{GT} + V_{photo}$$

For a given I_{GT} , a higher value for R1 and R2 will lead to a higher ripple across the Triac. In contrast to R1 and R2, a higher R_{GK} will reduce voltage ripple.

As an example, the Triac T810T-8FP ($I_{GT} = 10 \text{ mA}$, $V_{GT} = 1.3 \text{ V}$) is driven by phototriac "A" ($V_{TM} = 1.8 \text{ V typ.}$).

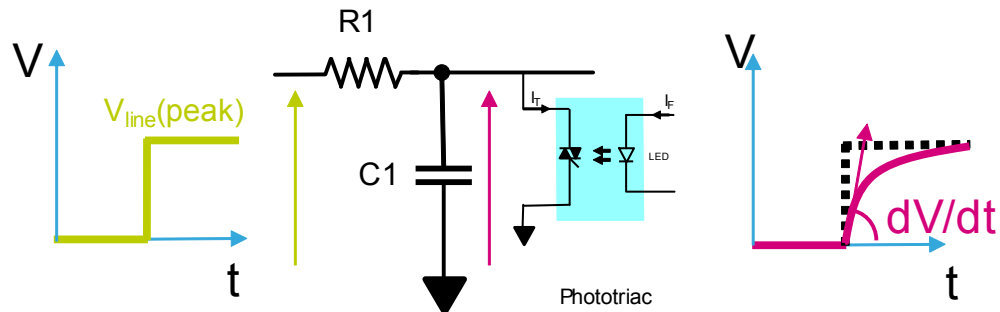
A maximum voltage ripple of 4 V is expected to avoid too much voltage ripple and a 390 Ω R_{GK} is chosen.

Neglecting V_{photo} in equation (4), this leads to:

$$R1 + R2 = 202.5 \Omega$$

Adopting standard values for resistors: $R2 = 150 \Omega$ and $R1 = 51 \Omega$

The last constraint is given by the rate of voltage rise across the phototriac. The worst case for the phototriac is represented by a sudden appearance of the peak line voltage at Triac turn-off (admittedly, an issue mainly present on inductive load). Using a simplified model neglecting circuit inductance, we find the maximum dV/dt across C1 capacitor.

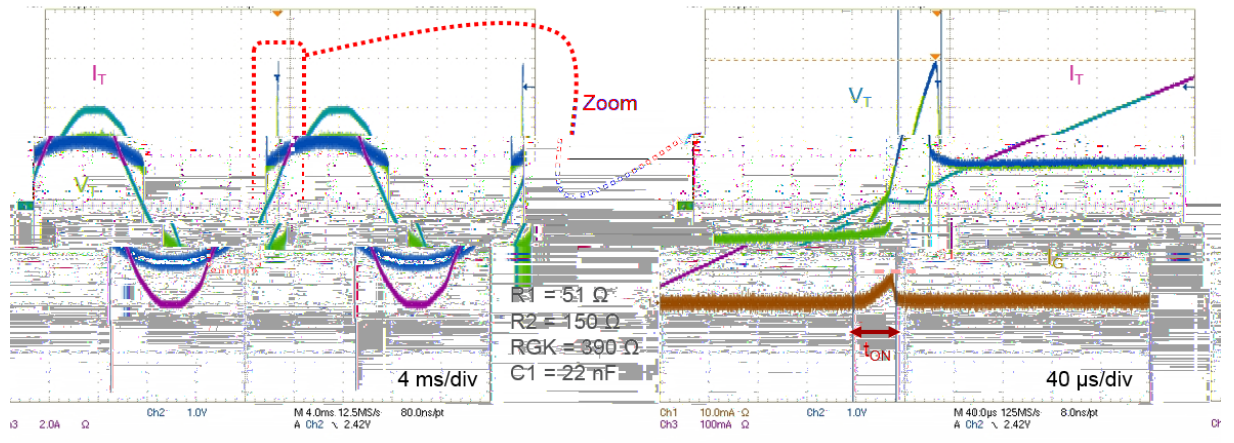


$$\frac{dV_{C1}}{dt} (\text{max}) = \frac{V_{line(peak)}}{\tau} = \frac{V_{line(peak)}}{R1 \times C1}$$

The critical rate of rise of off-state voltage for the phototriac A is 600 V/ μs , which gives a capacitance value for C1 of 10 nF. Taking into account the derating of static dV/dt with temperature (static dV/dt decreases when temperature increases), a capacitance of 22 nF is selected for C1.

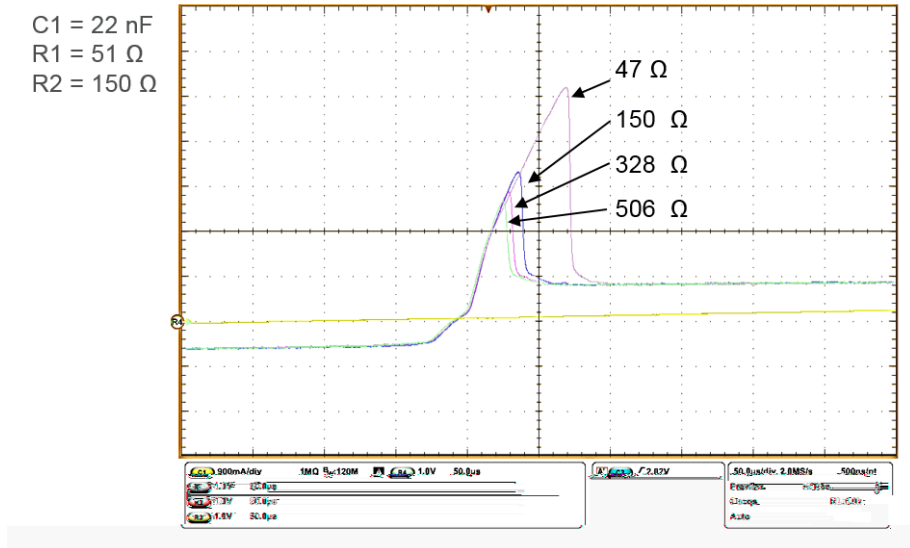
NETWORK	R1	R2	C	RGK
VALUE	51 Ω	150 Ω	22 nF	390 Ω

The Figure 14 shows voltage across a Triac (T810T-8FP) before turn-on for a 640 W resistive load. Line RMS voltage is 230 V / 50 Hz and power Triac is controlled with phototriac A. Values for drive circuit are given in Figure 13. A delay (t_{ON}) occurs between the zero current crossing point and the moment the power Triac triggers. The longer this t_{ON} , the higher V_T rises (see Figure 18). A high V_{TMAX} induces EMI noise which can be above the limit required by EN55014 standard (Figure 19).

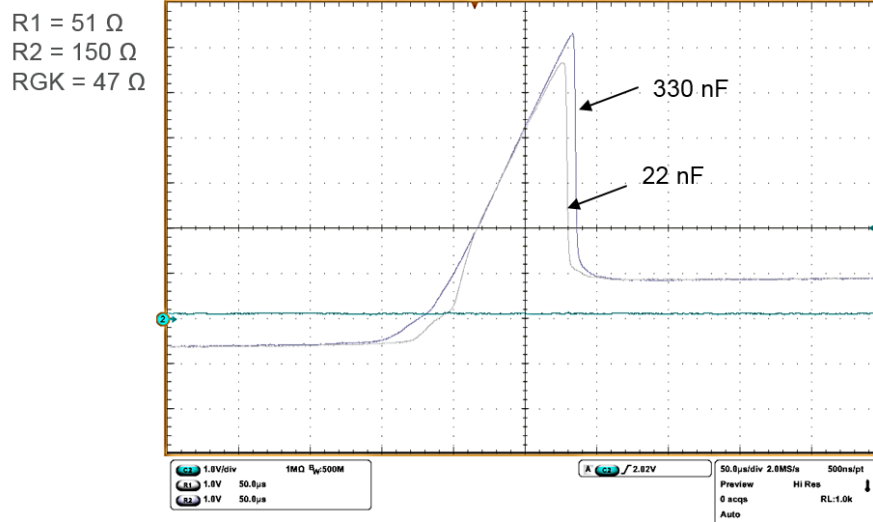


By varying the value of each element constituting the drive circuit, we can measure the impact of resistors and

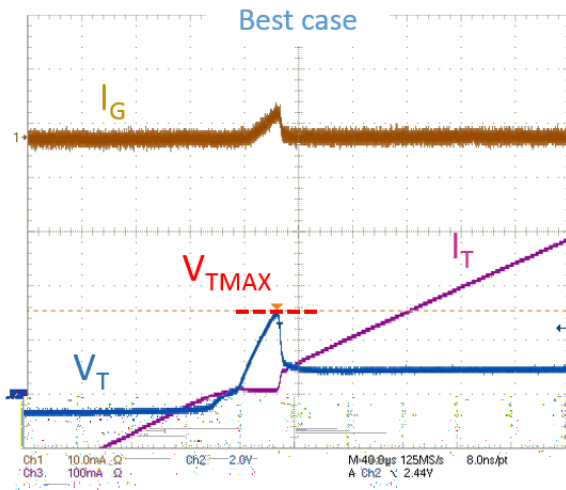
Influence of R_{GK} is further developed on Figure 16: reducing R_{GK} value leads to higher voltage ripple.



Snubber capacitor $C1$ also affects Triac peak voltage, but to a less extent than $R2$ or R_{GK} . A larger capacitor takes a longer time to charge which induces a corresponding higher voltage across Triac before turn-on.

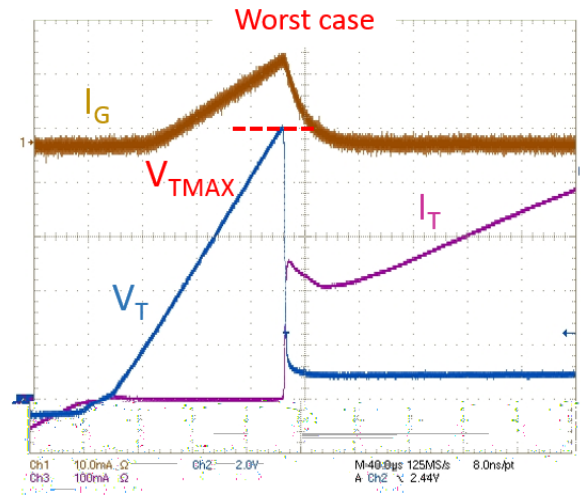


To illustrate the effect of voltage ripple on conducted EMI noise, two different configurations are selected. The first one can be considered as the best case: it shows a low V_{TMAX} of only 3.1 V. The second one represents the worst case with $V_{TMAX} = 10.1$ V.



$V_{TMAX} = 3.1$ V

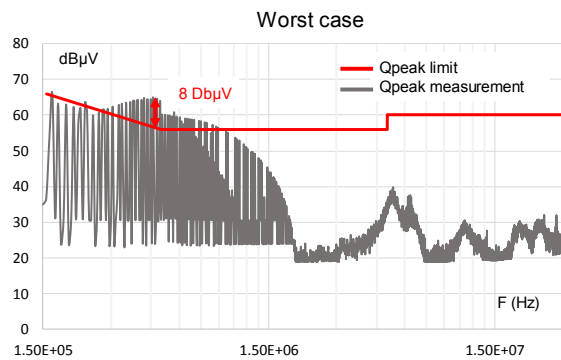
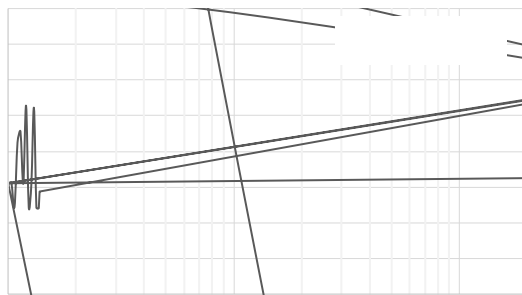
R1 = 51 Ω R2 = 150 Ω RGK = 390 Ω C1 = 22 nF



$V_{TMAX} = 10.1$ V

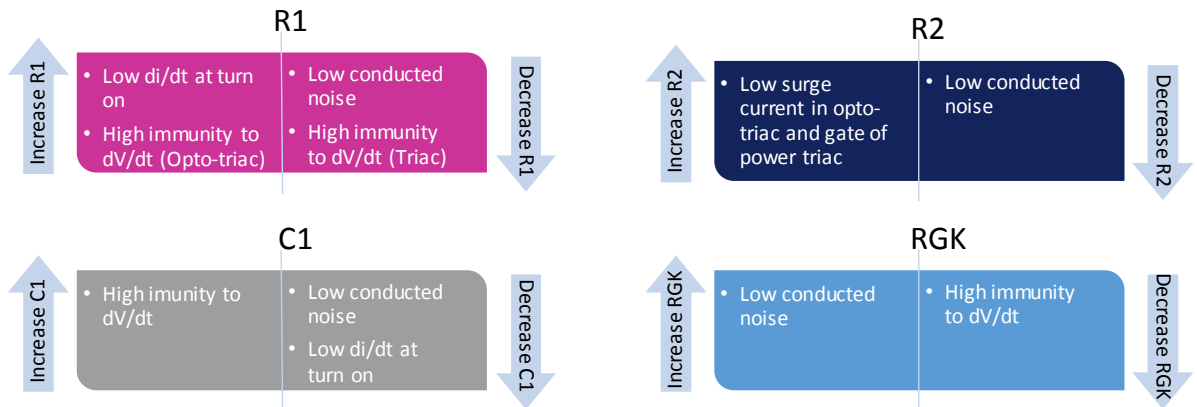
R1 = 51 Ω R2 = 390 Ω RGK = 51 Ω C1 = 330 nF

Resulting EMI noise is measured. For the first case (best case) measurement remains 5dB μ V below Q_{peak} limit (BE EN 55014-1: page 13 table 1): EN55014 test is passed. For the second case (worse case), quasi-peak measurement is 8 dB μ V above quasi-peak limit: the system is not compliant with EN55014 standard.



$V_{TMAX} = 10.1$ V R1 = 51 Ω R2 = 390 Ω RGK = 51 Ω C1 = 330 nF

There are compromise while choosing the right values for the resistors and capacitor of the drive circuit. To respect all the necessary constraints can lead to follow conflicting directions. For a good immunity to fast voltage transient and low EMI noise, it is recommended to reduce the value of R1 and R2. But a low value of R1 can result to high di/dt turn-on that may damage the power Triac, while a too low resistance for R2 cannot protect a phototriac against surge current. Likewise, a high snubber capacitance improves the Triac immunity against fast voltage transients but increases di/dt turn-on and conducted noise. At last low value for R_{GK} enhance static dV/dt rating but induces higher voltage across Triac at turn-on.

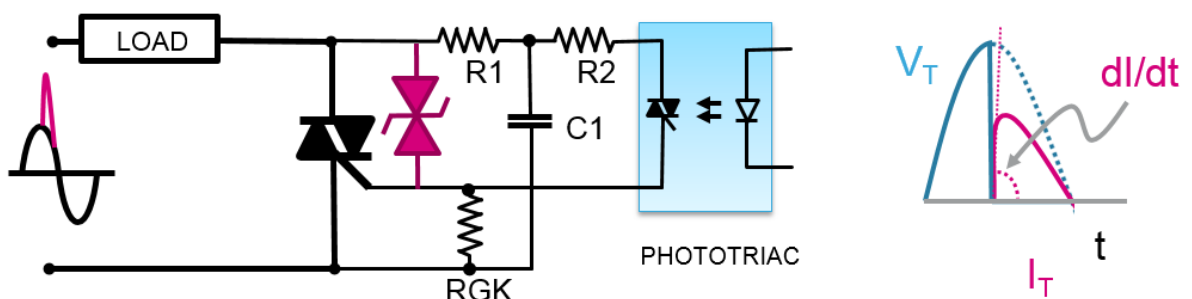


The validation of recommended values given in this application note must be done through experimental measurements according to application specifications.

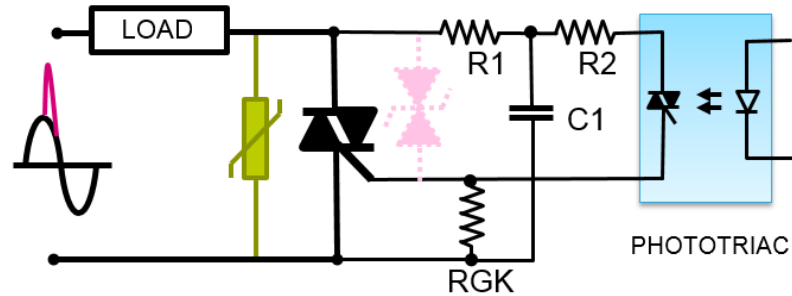
The ACST210 used previously belongs to the ACS/ACST switch family that is guaranteed to turn-on safely by break-over as long as the applied current stress is within the specified limits. So no overvoltage protection device is required in parallel to the device to protect it either from voltage surges coming from the mains or from an overvoltage generated at turn-off on inductive load.

But a standard Triac has to be protected from a voltage exceeding its maximum voltage capability.

One solution is to use a Transil connected across the Triac A2 and gate terminals as shown in [Figure 21](#). This solution allows to control accurately the maximum voltage applied to the Triac and the phototriac but leads to a spurious triggering of the device in case a surge is applied. If the load is resistive and surge occurs at peak mains voltage, the Triac turns on with very high di/dt that could cause its failure.



The second solution ([Figure 22](#)) is to add a metal-oxide varistor (MOV) in parallel to the AC switch terminals (for example, A1 and A2 for a Triac). It is adequate for resistive and capacitive loads and presents no di/dt issue.

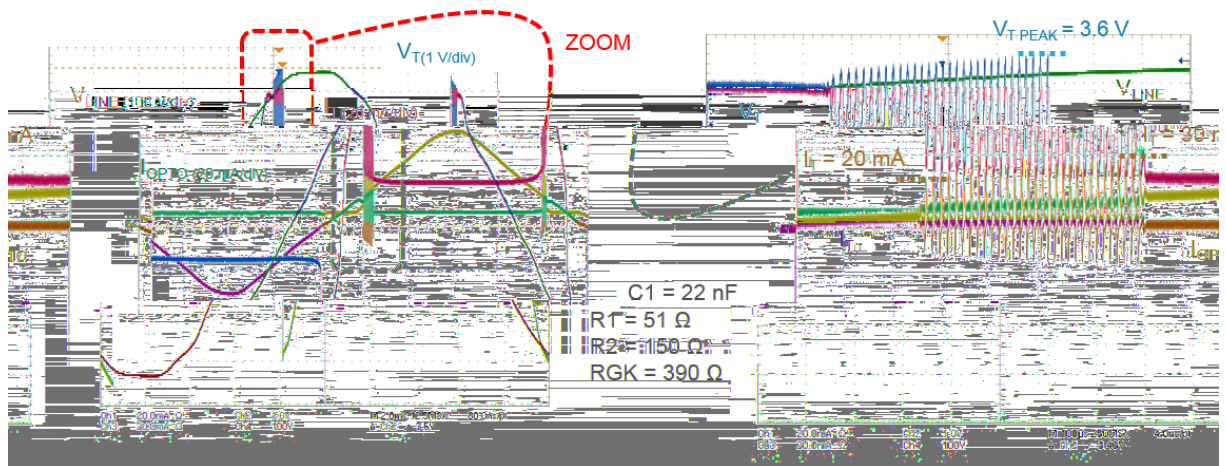


More details on overvoltage protection can be found in AN4363 §2.3.

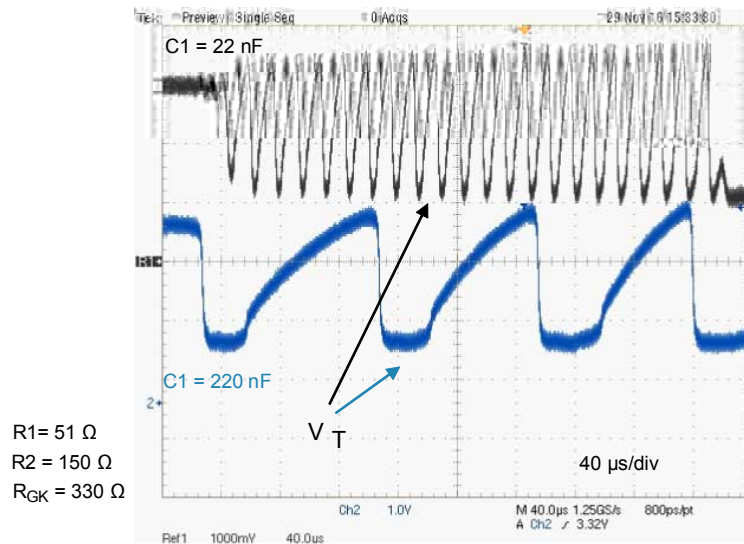
The phototriac / Triac association works well with high-power resistive loads where the load current increases fast at Triac turn-on and so reaches the latching current I_L (refer to AN303) during the transient turn-on.

But with highly inductive load, or very low RMS current load, the current passing through the load may be too close to Triac latching current I_L and can lead to oscillations at turn-on.

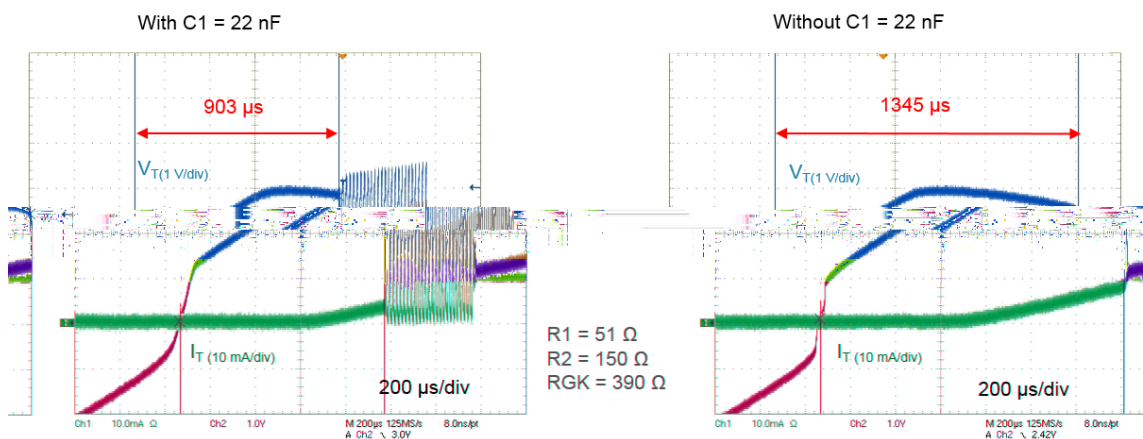
To illustrate this issue an inductive load ($L_{load} = 10\text{ H}$, $R_{load} = 5.9\text{ K}\Omega$) is used with an ACST210-8 controlled by phototriac "A". Power supply is 230 V / 50 Hz.



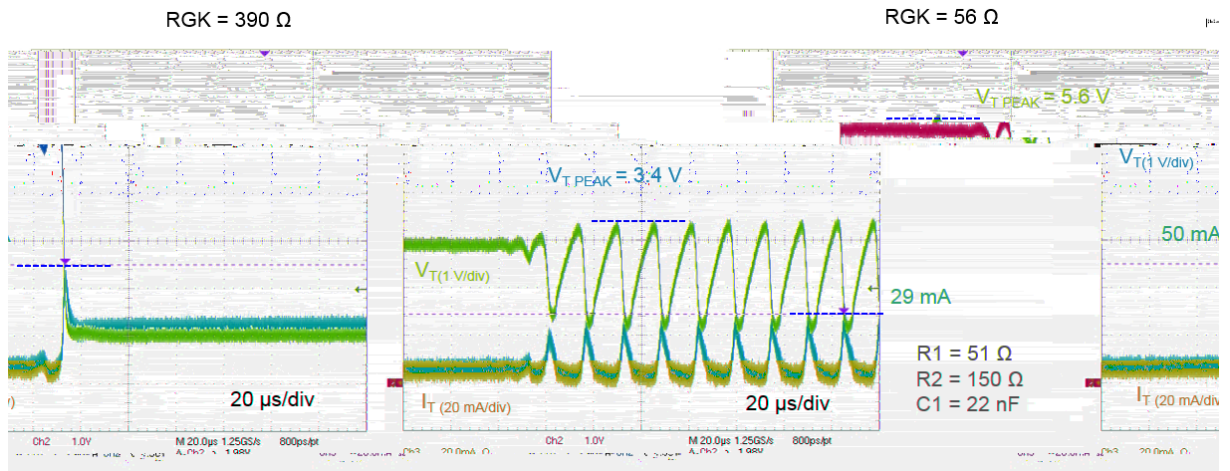
At turn-on, the voltage A2-A1 across the Triac decreases, carrying a corresponding fall of the gate current since this gate current is generated by voltage drop A2-A1. If the load current is too small, the latching current (I_L) is not reached and Triac turns off: the voltage is reapplied across A2 and A1. A gate current is generated and the Triac is turned on again. The whole process is repeated again and again until the latching current is reached, producing eventually EMI noises.



As shown on Figure 24, the frequency of circuit oscillation is dependent on $C1$ capacitor value. The 220 nF case is only given here to emphasize the frequency shift with capacitor changes. It is not a value that should be used with a low current load as capacitive current drawn by such a large and lossy snubber would drive the load permanently no matter the state of the Triac.



With the snubber capacitor removed, oscillations stop. Turn-on of the Triac occurs later than with a capacitor (1.3 ms against 0.9 ms), giving time to Triac current (I_T) to reach latching current (I_L).



A lower R_{GK} sinks a higher current out from the gate, thus turn-on happens later with a higher V_T . This higher voltage and the induced higher I_T at turn-on allows a better latch-up with no oscillations.

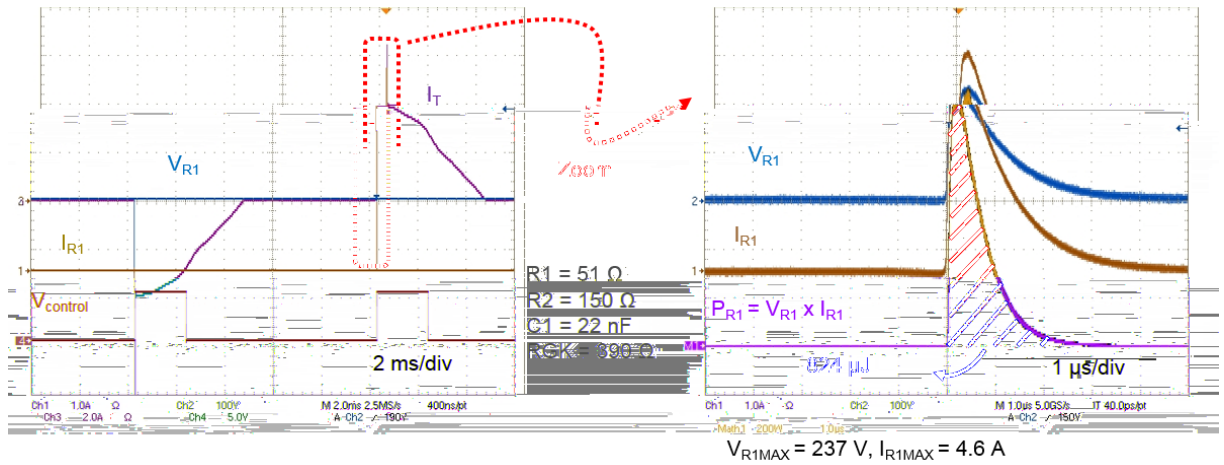
Using a snubber capacitor on low power or highly inductive loads leads to circuit oscillations. Eliminating the snubber capacitor avoids bounces, but cannot be recommended as it decreases dV/dt immunity. A lower R_{GK} keeps off bounces and improves dV/dt withstanding, but increases EMI noise. Once again, as already discussed for EMI noise on resistive load, choosing the right value for the drive circuit requires an empirical approach to adjust values recommended in this application note.

Once the values of the drive network are chosen, one problem remains: what must be the voltage and power rating of resistor and capacitor composing the network?

The case of R_{GK} is rather straightforward: since it is connected in parallel with gate-A1 junction, its voltage always remains below V_{GT} . The current flowing through the resistance is limited to V_{GT} divided by R_{GK} plus part of gate parasitic capacitive current bypassed by this resistance.

Capacitance $C1$ is submitted to supply voltage: it must be specified to stand up peak supply voltage plus at least a 15% margin.

$R1$ and $R2$ require more care. A worst case scenario is chosen to study the maximum voltage and current they have to handle. A random phase phototriac is used with a T810T-8FP to drive a 640 W resistive load connected to a 230 V 50 Hz main supply. A power Triac turns on at AC peak voltage when $C1$ voltage is maximum (the phase shift is negligible).



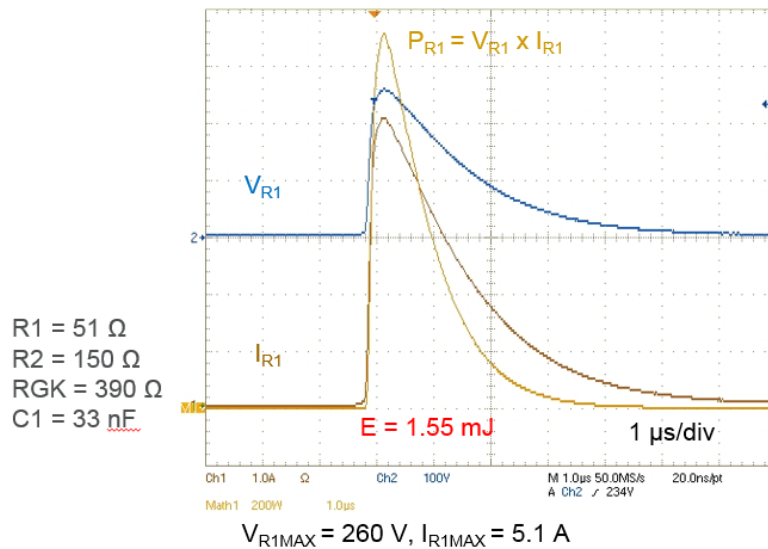
At main Triac turn-on, C1 capacitor discharge leads to a peak current of 4.6 A through R1, while the voltage across R1 reaches 237 V. Corresponding energy is $E = 824 \mu\text{J}$, which is approximately the energy stored within C1 capacitor:

$$E_{C1} = \frac{1}{2} CV^2 = 1164 \mu\text{J}, \text{ with } V = 230 \sqrt{2} \text{ and } C = 22 \text{ nF}$$

Since this pulse occurs every 10 ms, average power is:

$$P = E/10 \text{ ms} = 0.08 \text{ W}$$

A $\frac{1}{4} \text{ W}$ resistor with 400 V rating is suitable for R1.

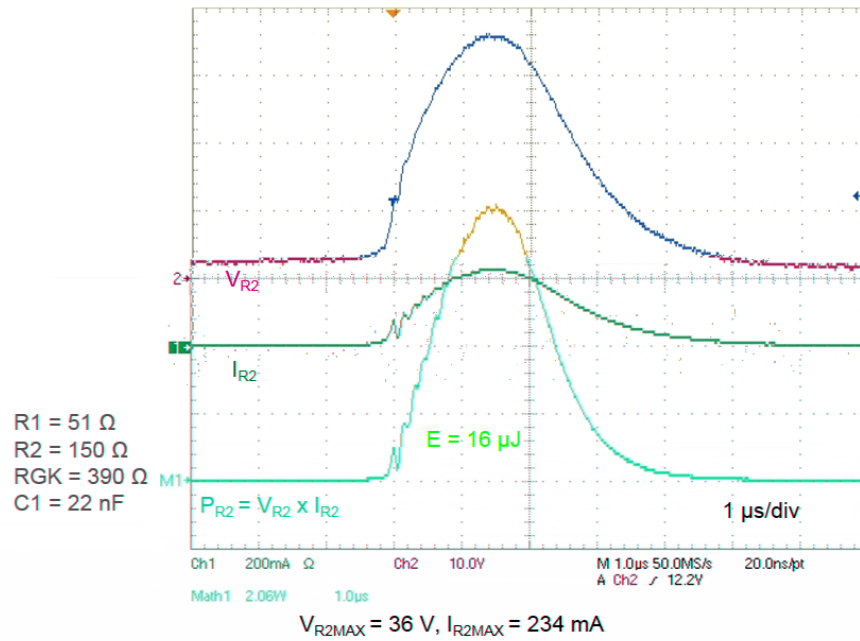


A designer may face the problem in another way: what is the highest capacitance $C_{\frac{1}{4}W}$ for which a $\frac{1}{4} \text{ W}$ resistor is still fitting?

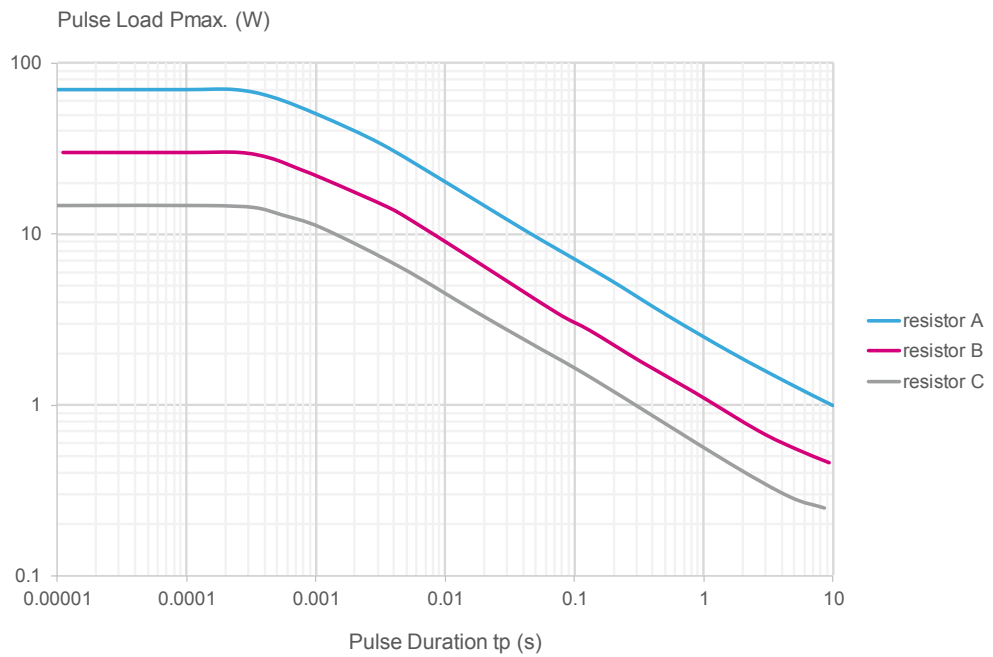
$$C_{\frac{1}{4}W} = 0.01 \times 2 \times P/V^2 = 47 \text{ nF}, \text{ with } P = 0.25 \text{ W and } V = 230 \sqrt{2}$$

if the snubber capacitance C1 is above 47 nF, then a $\frac{1}{2} \text{ W}$ resistor has to be used (230 V mains).

With almost all the capacitive energy dissipated in R1, R2 sustains less constraints. In the same conditions (turn-on at AC peak voltage), the peak current is only 234 mA, representing a low energy of 16 μJ . A $\frac{1}{4}$ W resistor is good enough for any configuration.



The computation on R1 and R2 values is based on the average power specification of the resistor, which is often the only data about power rating in resistor datasheets. Nevertheless, resistors must be able to withstand the pulse energy for short duration times. With $C1 = 33 \text{ nF}$, the capacitor discharge yields a peak power of 1300 W (Figure 28). Figure 30 shows an example of derating of pulse power versus pulse duration. The maximum allowed peak power reaches a constant value for $t_p < 200 \mu\text{s}$ where the heat flow out of the resistor is very slow compared to the pulse duration. This graph, unfortunately very rarely available, is extremely worthwhile to choose the right resistor.

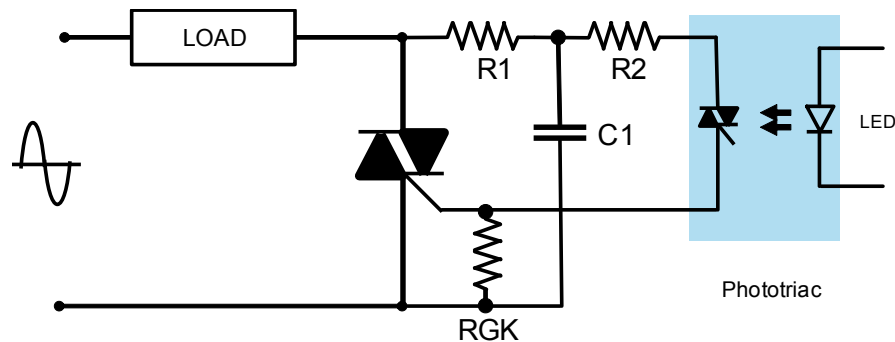


When it comes to AC-switching, Triacs rule the domain of solid-state power switching exclusively. In many commercial and industrial applications, they represent the simplest and most robust solution existing today.

The phototriac has been forming a succeeding combination with Triac for a long time: it provides uncomplicated safety isolation from the high voltage since it does not require an auxiliary supply referenced to the mains.

As shown in this document, phototriac performance cover a very large range and can have a bad influence on dV/dt immunity. First step when designing a new Triac application with a phototriac is to choose carefully the right part number.

Implementing a snubber network can help to reduce the three drawbacks brought by phototriac drive: EMI noise, low immunity and oscillations at turn-on. This snubber must be carefully chosen to avoid high dI/dt created by capacitor discharge that would destroy the Triac or the phototriac. Recommended values, given in Figure 31, constitute a good starting base that can be adjusted afterwards according to experimental measurements.



Drive Network	Recommended value	Associated range
R1	51 Ω	47 Ω to 620 Ω
R2	150 Ω	47 Ω to 150 Ω
RGK	390 Ω	50 Ω to 390 Ω
C1	22 nF	22 nF to 47 nF

Further information can be found in the following application notes:

AN4903: How to implement a SCR or a Triac in a hybrid relay application?

AN3168: Non-insulated SCRs / Triacs control circuits

AN4606: Inrush-current limiter circuits (ICL) with Triacs and thyristors (SCR) and controlled bridge design tips

AN437: RC snubber circuit design

AN303: Latching current

AN439: Snubberless™ and logic level Triac behavior at turn-off

AN1379: Z01 and ACS behavior compared under fast voltage transients

AN2986: AC switch triggering with 3.3 v power supply

AN4363: How to select the Triac, ACS, or ACST that fits your application



07-Nov-2018	1	Initial release.
10-Jul-2020	2	Updated Section 3.3.1 and Section 3.6 .

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